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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/749,590	12/28/2000	Fumio Ohtake	001752	4831

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EXAMINER
MAI, ANH D

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/749,590	Applicant(s) OHTAKE ET AL.	
	Examiner Anh D. Mai	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *11-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 11, 2003 has been entered.

Amendment

2. Amendment filed March 11, 2003 has been entered as Paper No. 13. Claims 1-4 have been amended. Claims 18 and 19 have been cancelled. Claims 1-17 are pending. Claims 11-17 have been withdrawn.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 2, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over K. Kasai et al. *W/WN$_x$/Poly-Si Gate Technology for Future High Speed Deep Submicron CMOS LSIs*, in view of Jeng et al. (U.S. Patent No. 5,877,074) all of record.

With respect to claims 1 and 2, Kasai teaches a semiconductor device substantially as claimed including:

a pair of impurity diffused regions formed in a silicon substrate, spaced from each other; and

a gate electrode formed above the silicon substrate between the pair of impurity diffused regions with a gate insulation film interposed therebetween, the gate electrode being formed of a first polycrystalline silicon film formed on the gate insulation film, a second polycrystalline silicon film formed on the first polycrystalline silicon film and having crystal grain boundaries which are discontinuous to the first polycrystalline silicon film, and a metal nitride film (WN_x) formed on the second polycrystalline silicon film, and a metal film (W) formed on the metal nitride film. (See Fig. 2).

Thus, Kasai is shown to teach all the features of the claim with the exception of the second polycrystalline silicon film having a thickness and thinner than that of the first polycrystalline silicon film. Note that, the claimed thickness does not appear to be critical.

Note that the specification contains no disclosure of either the *critical nature of the claimed dimension of any unexpected results arising therefrom*. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

However, Jeng teaches a semiconductor device including: a gate electrode formed above the silicon substrate (11) with a gate insulation film (12) interposed therebetween, the gate electrode being formed of a first polycrystalline silicon film (31) formed on the gate insulation film (12), a second polycrystalline silicon film (32) formed on the first polycrystalline silicon film (31), having a thickness of that includes the upper limit of claimed range, 20 nm, and is thinner than that of the first polycrystalline silicon film (31). (See Fig. 5, col. 3, ll. 5-19).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the second polycrystalline silicon film (32) of Kasai to the thickness of 20 nm, as taught by Jeng to prevent impurity atoms from penetration during the formation of the metal layer (W).

Regarding the second polycrystalline silicon film, the α-Si of the references are subjected to a high temperature anneal, thus, crystallized, hence polycrystalline silicon. Further, since the α-Si is formed at a lower temperature than that of the polysilicon (first) layer, thus, the grain size is differed than that of polysilicon, therefore, the crystal grain boundary of the two layer are discontinuous. The subject matter is well known in the art. (See Jeng '074, col. 3, ll. 5-19).

With respect to claims 5 and 6, the first polycrystalline silicon film of Kasai further includes boron.

4. Claims 3, 4 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai et al. and Jeng '074 as applied to claims 1 and 2 above, and further in view of Tsukamoto (U.S. Pub. No. 2001/0000629) (of record).

With respect to claims 3 and 4, Kasai and Jeng teaches a gate electrode formed above the semiconductor substrate including the second polycrystalline silicon film formed on the first polycrystalline silicon film.

Thus, Kasai and Jeng are shown to teach all the features of the claim with the exception of explicitly disclosing an oxide film formed between the first and second polycrystalline silicon films.

However, Tsukamoto teaches a native oxide film (20) is formed between the first (6) and second (7) polycrystalline silicon film so that the grain size of the second polycrystalline silicon film (7) can become large. (See Fig. 6).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form an oxide film between the first and second polycrystalline silicon films of Kasai as taught by Tsukamoto to suppress fluctuation in the threshold voltage V_{th}.

Product by process limitation:

The expression "or a chemical oxide film formed by liquid chemical treatment" is taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

With respect to claims 7 and 8, the first (6) and second (7) polycrystalline silicon film of Tsukamoto are further doped with boron. Further, the native oxide layer (20) formed between the two polycrystalline silicon films (6, 7) functions as impurities diffusion blocker (suppress fluctuations in the threshold voltage V_{th} caused by mutual diffusion of the impurities) and following an anneal step, the impurities are known to segregate toward the upper surface, therefore, the boron concentration in the first polycrystalline silicon film (6) near the interface between the first polycrystalline silicon film (6) and the second polycrystalline silicon film (7) is higher than boron concentration in the second polycrystalline silicon film (7) near an interface between the first polycrystalline silicon film (6) and the second polycrystalline silicon film (7).

With respect to claims 9 and 10, the crystal grain size of the first polycrystalline silicon film (6) of Tsukamoto is smaller than that of the second polycrystalline silicon film (7).

Response to Arguments

5. Applicant's arguments with respect to claims 1-10 have been fully considered but are persuasive.

In response to applicant's argument that Jeng '074 is nonanalogous art, it has been held that a prior art reference must *either be in the field* of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, both Kasai and Jeng '074 teach a **semiconductor device** having two polysilicon layers comprising discontinuous grain boundary.

With respect to "polycide gate" or "polymetal gate" these are variations of a Field Effect Transistor (FET).

Since Jeng teaches the thickness of second polysilicon (32) that includes the claimed range, the combination of the references clearly renders claims 1, 2, 5 and 6 obvious.

With respect to claims 3, 4 and 7-10, since claims 1 and 2 are obvious over Kasai et al. and Jeng, the dependent claims 3, 4 and 7-10 are obvious for the same reason discussed above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
April 29, 2003

LONG PHAM
PRIMARY EXAMINER